SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
Siddharth Nagar, Narayanavanam Road – 517583
QUES TION BANK (DESCRIPTIVE)

Subject with Code: DIGITAL CIRCUITS DESIGN (23EC0403)
Course & Branch: B. Tech –ECE
Year & Semester: II - B. Tech. & I-Semester **Regulation:** R23

UNIT- I

BOOLEAN ALGEBRA, LOGIC OPERATIONS, AND MINIMIZATION OF BOOLEAN FUNCTIONS

PART-A (2 MARKS)

1.	**(a)**	List out the types of number systems with one example for each.	**[L2][CO1]**	**[2M]**
	(b)	Convert $(41.6875)_{10}$ to Hexadecimal number.	**[L5][CO1]**	**[2M]**
	(c)	Write the truth table for F=(A+B)(C+D)	**[L2][CO1]**	**[2M]**
	(d)	What are Universal Gates? Give their truth tables.	**[L1][CO1]**	**[2M]**
	(e)	Perform the following Subtraction using 10's complement method. i) 3456 – 245 ii) 631-745	**[L1][CO1]**	**[2M]**

PART-B (10 MARKS)

2.	**(a)**	Convert the following numbers: i) $(AB)_{16}=(\quad)_2$ ii) $(1234)_8=(\ )16$ (iii) $(1000011)_2 = (\ )_{10}$	**[L5][CO1]**	**[5M]**
	(b)	Convert the following to binary and then to gray code. i) $(AB33)_{16}$ ii) $(BC54)_{16}$	**[L5][CO1]**	**[5M]**
3.		Convert the following: a) $(1AD)_{16}=(\ )_{10}$ b) $(453)_8=(\ )_{10}$ c) $(10110.0101)_2=(\ )_{10}$ d) $(5436)_{10}=(\ )_{16}$ e) $(647)_{10}= (\ )_8$	**[L6][CO1]**	**[10M]**
4.	**(a)**	Perform the following subtraction by using 1's complement. i) 111001-1010 ii) 0011-10001	**[L1][CO1]**	**[5M]**
	(b)	Explain about the Binary Codes in detail.	**[L1][CO1]**	**[5M]**
5.	**(a)**	Prove De Morgan's theorems using Perfect Induction Method.	**[L3][CO1]**	**[5M]**
	(b)	Simplify the given boolean expression: $f = AB + A\bar{B}(\overline{\bar{A}\bar{C}})$	**[L3][CO1]**	**[5M]**
6.	**(a)**	Simplify the given Boolean expression to a sum of 3 terms. A'C'D' +AC' +BCD + A'CD' + A'BC + AB'C'	**[L4][CO2]**	**[5M]**
	(b)	Realize the following Boolean function using minimum number of logic gates. $f = \bar{x}\bar{y}z + \bar{x}yz + x\bar{y}\bar{z} + x\bar{y}z$	**[L4][CO2]**	**[5M]**
7.		Obtain the Dual and complement to the following Boolean expressions. (i) AB'C+AB'D+A'B' (ii) A'B'C+ABC'+A'B'C'D	**[L1][CO2]**	**[10M]**
8.		Illustrate the digital logic gates with graphical symbol, algebraic function and truth table.	**[L2][CO1]**	**[10M]**
9.		Express the following Boolean functions into Canonical form. i) F1=AB+BC+CA ii) F2= XY+Z+YZ+XYZ	**[L2][CO2]**	**[10M]**

10.	**(a)**	Simplify the expression f(x, y, z)= Σ (0,1,2, 3, 6, 7)	**[L4][CO3]**	**[5M]**
	(b)	Obtain the simplified SOP and POS form of the following boolean expression, Y= B C + A C' +A B + A B C using K-map.	**[L1][CO3]**	**[5M]**
11.	**(a)**	Simplify the Boolean expression, F=A'+AB+ABD'+AB'D'+C' using Four Variable K-Map and draw the logic diagram using AOI logic.	**[L4][CO3]**	**[5M]**
	(b)	Simplify the expression in S O P form using don't cares. Y= Σ (4,5,6,8,9) + d Σ (3, 7, 10,11,14,15)	**[L4][CO3]**	**[5M]**

UNIT- II

COMBINATIONAL LOGIC CIRCUITS

PART-A (2 MARKS)

1.	**(a)**	Define a Combinational Circuit and draw its block diagram.	**[L1][CO4]**	**[2M]**
	(b)	Define the following: i) Half adder and ii) Full Adder	**[L1][CO4]**	**[2M]**
	(c)	List the applications of encoder and decoder.	**[L1][CO4]**	**[2M]**
	(d)	What is a Priority encoder?	**[L1][CO4]**	**[2M]**
	(e)	Define Multiplexer and Demultiplexer.	**[L1][CO4]**	**[2M]**

PART-B (10 MARKS)

2.	**(a)**	Explain the procedure of designing a combinational logic circuit with an example.	**[L2][CO4]**	**[5M]**
	(b)	Design & implement Half Adder and Half subtractor logic circuits using AOI logic.	**[L3][CO4]**	**[5M]**
3.	**(a)**	Define a Full Adder and realize Full Adder circuit using two half adders.	**[L3][CO4]**	**[5M]**
	(b)	Design a Full Subtractor using truth table and realize Full subtractor circuit using two half subtractors.	**[L3][CO4]**	**[5M]**
4.	**(a)**	Design a 4 bit parallel adder/ Subtractor using full adders.	**[L3][CO4]**	**[4M]**
	(b)	Design & implement a 4-bit Binary-to-BCD code converter.	**[L3][CO4]**	**[6M]**
5.	**(a)**	Design & implement a 4-bit BCD -to-Excess-3 code converter.	**[L3][CO4]**	**[5M]**
	(b)	Construct a BCD Adder-circuit using 4-bit binary adders.	**[L3][CO4]**	**[5M]**
6.	**(a)**	Explain the working of a Carry- Look ahead adder with a neat logic diagram.	**[L2][CO4]**	**[5M]**
	(b)	Explain about Binary multiplier and realize its logic diagram.	**[L2][CO4]**	**[5M]**
7.	**(a)**	What is a Magnitude comparator? Design a 1-bit magnitude comparator and explain.	**[L1][CO4]**	**[4M]**
	(b)	Analyze the operation of a 2-bit magnitude comparator and derive the Boolean expressions for its outputs.	**[L4][CO4]**	**[6M]**
8.	**(a)**	What is encoder? Design an octal to binary encoder.	**[L3][CO4]**	**[5M]**
	(b)	Define Decoder and explain in detail about a 2 to 4 line binary decoder.	**[L2][CO4]**	**[5M]**
9.	**(a)**	Draw the circuit for 3 to 8 decoder and explain.	**[L2][CO4]**	**[5M]**
	(b)	Implement the full adder with decoder and two OR gates		
10.	**(a)**	Define Multiplexer. Construct 4:1 multiplexer with logic gates and truth table.	**[L3][CO4]**	**[5M]**
	(b)	Represent the following Boolean function with an 8:1 multiplexer. F(A,B,C,D) = A'BD'+ACD+B'CD+A'C'D.	**[L2][CO4]**	**[5M]**
11.	**(a)**	Implement the following Boolean function using 8:1 MUX f(P,Q,R,S) = Σ (0,1,3,4,8,9,15)	**[L3][CO4]**	**[5M]**
	(b)	What is Demultiplexer? Design an 1:8 demultiplexer using two 1:4 demultiplexers.	**[L3][CO4]**	**[5M]**

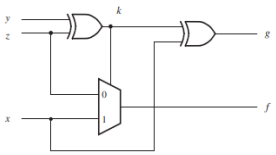
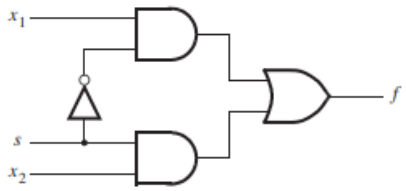
UNIT- III

HARDWARE DESCRIPTION LANGUAGE

PART-A (2 MARKS)

1.	**(a)**	Differentiate between Verilog and VHDL.	**[L4][CO6]**	**[2M]**
	(b)	Define the structural and behavioral representation of logic circuits.	**[L1][CO6]**	**[2M]**
	(c)	Explain about the module representation of logic circuits in Verilog.	**[L1][CO6]**	**[2M]**
	(d)	What are Verilog parallel case and full case statements?	**[L2][CO6]**	**[2M]**
	(e)	What is the Sensitivity list?	**[L1][CO6]**	**[2M]**

PART-B (10 MARKS)

2.	a) What is the syntax used to write a Verilog Code?	**[L1][CO6]**	**[4M]**
	b) Write Verilog code to implement the following function: f (x1, x2, x3) =∑ m(0, 1, 3, 4, 5, 6) using the continuous assignment.	**[L1][CO6]**	**[6M]**
3.	Explain about the Hierarchial Verilog code with an example.	**[L1][CO6]**	**[10M]**
4.	a) Write a Verilog code to implement the function, f (x1, x2, x3) = m(1, 2, 3, 4, 5, 6) using the gate-level primitives. Ensure that the resulting circuit is as simple as possible.	**[L1][CO6]**	**[5M]**
	b) Write Verilog code that represents the logic circuit shown in Figure below. Use only continuous assignment statements to specify the required functions. 	**[L1][CO6]**	**[5M]**
5.	a) Write Verilog code for the following logic circuit diagram using behavioral structure representation. 	**[L1][CO6]**	**[5M]**
	b) Write an Verilog code for Half Adder and Full Subtractor with the help of Truth tables.	**[L1][CO6]**	**[5M]**
6.	Write Verilog code to implement the Boolean function F=A'+AB+ABD'+AB'D'+C'	**[L1][CO6]**	**[10M]**
7.	a) Write an Verilog code for Full Adder with the help of Truth table.	**[L1][CO6]**	**[5M]**
	b) Design an BCD adder and write the code for it in Verilog.	**[L4][CO6]**	**[5M]**
8.	a) Explain Conditional operator in Verilog with an example.	**[L2][CO6]**	**[5M]**
	b) Explain if-else statement in Verilog with an example.	**[L2][CO6]**	**[5M]**
9.	a) State the importance of CAD Tools in HDL.	**[L1][CO6]**	**[5M]**
	b) Explain case statement in Verilog with an example.	**[L2][CO6]**	**[5M]**
10.	Write an Verilog code for 2 Bit binary multiplier in structural Model.	**[L1][CO6]**	**[10M]**
11.	a) Write an Verilog code for 16x1 MUX in behavioral Model.	**[L1][CO6]**	**[5M]**
	b) State For loop statement in Verilog and explain the same with an example.	**[L1][CO6]**	**[5M]**

UNIT- IV
SEQUENTIAL LOGIC CIRCUITS

PART-A (2 MARKS)

1.	**(a)**	List the differences between Latch and Flip-flop.	**[L4][CO4]**	**[2M]**
	(b)	What is race around condition?	**[L1][CO4]**	**[2M]**
	(c)	Define a sequential circuit and draw its block diagram.	**[L1][CO4]**	**[2M]**
	(d)	List the applications of T flip flop.	**[L1][CO4]**	**[2M]**
	(e)	What is a Register?	**[L1][CO4]**	**[2M]**

PART-B (10 MARKS)

2.	a) Define a sequential logic circuit and sketch its block diagram.	**[L1][CO4]**	**[3M]**
	b) Differentiate between combinational and sequential circuits.	**[L2][CO4]**	**[3M]**
	c) Differentiate between synchronous and asynchronous sequential circuits.	**[L2][CO4]**	**[4M]**
3.	a) Define Latch and list different types of Latches.	**[L1][CO4]**	**[3M]**
	b) Define Flip-Flop. What are the different types of Flip-Flops?	**[L1][CO4]**	**[3M]**
	c) Explain the working principle of RS Flip-Flop with the help of logic diagram and give its Characteristic Table and Graphic symbol.	**[L2][CO4]**	**[4M]**
4.	a) With the help of logic diagram, obtain the characteristic table of D & T Flip-Flops. Also draw their graphic symbols.	**[L2][CO4]**	**[5M]**
	b) Explain the working principle of JK Flip-Flop in detail. Also give its characteristic equation, Graphic symbol and Excitation equation.	**[L2][CO4]**	**[5M]**
5.	a) Convert SR flip flop into JK Flip-Flop. Draw and explain its logic diagram.	**[L2][CO4]**	**[5M]**
	b) Design T Flip Flop using JK Flip-Flop and explain its logic diagram.	**[L3][CO4]**	**[5M]**
6.	a) Derive the excitation tables for SR, D, JK, and T Flip-Flops.	**[L3][CO4]**	**[5M]**
	b) Explain about the Ring counter in detail.	**[L2][CO4]**	**[5M]**
7.	a) Explain about the Johnson counter in detail.	**[L2][CO4]**	**[5M]**
	b) Define a counter and design a 4-bit Ripple counter.	**[L1][CO4]**	**[5M]**
8.	Design a 4 bit Decade counter.	**[L4][CO4]**	**[10M]**
9	What is a synchronous counter? Design a 3-bit synchronous up/down counter.	**[L4][CO4]**	**[10M]**
10.	Define a Shift register and explain its types.	**[L2][CO4]**	**[10M]**
11.	a) Write an Verilog code for 4- bit ring counter	**[L1][CO6]**	**[5M]**
	b) Design an 2-bit synchronous up-counter using Verilog Code.	**[L6][CO6]**	**[5M]**

UNIT- V
FINITE STATE MACHINES AND PROGRAMMABLE LOGIC DEVICES

PART-A (2 MARKS)

1.	**(a)**	What are the differences between Moore and Mealy Machines?	**[L1][CO2]**	**[2M]**
	(b)	List some of the limitations of finite state machines.	**[L1][CO2]**	**[2M]**
	(c)	State the types of ROM.	**[L1][CO5]**	**[2M]**
	(d)	List the major differences between PLA and PAL.	**[L1][CO5]**	**[2M]**
	(e)	List basic types of programmable logic devices.	**[L1][CO5]**	**[2M]**

PART-B (10 MARKS)

2.	a) Define Mealy model and explain it with neat diagram.	**[L1][CO2]**	**[3M]**
	b) Define Moore model. Explain it with neat diagram.	**[L1][CO2]**	**[3M]**
	c) Distinguish between Mealy & Moore machines.	**[L2][CO2]**	**[4M]**
3.	Explain the following related to sequential circuits with suitable examples: a) State diagram b) State table c) State assignment	**[L2][CO2]**	**[10M]**

4.	Derive the simplified sequential circuit for the following state table. PS | Next State (X=0, X=1) | Output (X=0, X=1) A: a, b, 0, 0 B: c, d, 0, 0 C: a, d, 0, 0 D: e, f, 0, 1 E: a, f, 0, 1 F: g, f, 0, 1 G: a, f, 0, 1	**[L3][CO2]**	**[10M]**
5.	Determine the minimal state equivalent of the state table given. PS | Next State (X=0, X=1) | Output (X=0, X=1) A: a, b, 0, 0 B: c, g, 0, 1 C: a, d, 0, 0 D: e, f, 0, 1 E: c, g, 0, 1 F: a, b, 0, 0 G: E, f, 0, 1	**[L3][CO2]**	**[10M]**
6.	Explain and Design a Sequence Detector.	**[L2][CO5]**	**[10M]**
7.	Explain in brief about Programmable Read Only Memory (PROM) with a suitable example.	**[L2][CO5]**	**[10M]**
8.	Illustrate the PLA for the following Boolean function. (i) $F_1 = \Sigma m(0,1,3,4)$ (ii) $F_2 = \Sigma m(1,2,3,4,5)$.	**[L3][CO5]**	**[10M]**
9.	Illustrate PLA for the following Boolean function. $F_1(A,B,C) = \Sigma m(3,5,7)$ $F_2(A,B,C) = \Sigma m(1,2,3,7)$	**[L3][CO5]**	**[10M]**
10.	Illustrate the PAL for the following Boolean functions. (i) $A(w,x,y,z) = \Sigma m(0,2,6,7,8,9,12,13)$ (ii) $B(w,x,y,z)) = \Sigma m(0,2,6,7,8,9,12,13,14)$	**[L3][CO5]**	**[10M]**
11.	a) Draw and Briefly explain the basic structures of CPLD & FPGA	**[L2][CO5]**	**[5M]**
	b) Compare PROM,PLA & PLA	**[L2][CO5]**	**[5M]**